1 WX1820AL

WX1820AL

CPU CPU CPU

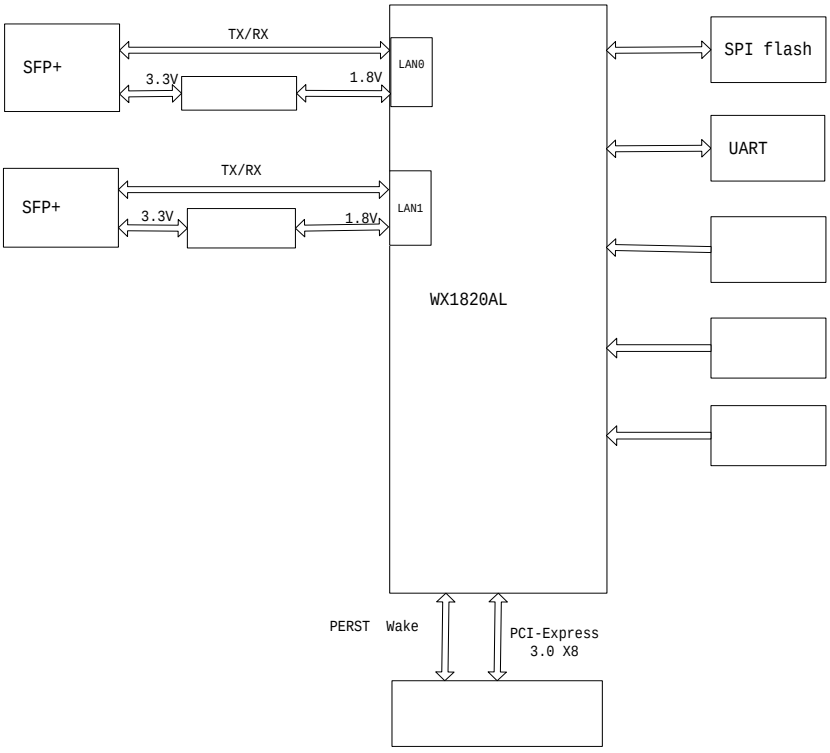
WX1820AL 300

PCI Express X8

I/O

WX1820AL MAC SFP+

WX1820AL



1.1

1.1.1

- 10G SFI/KR/XAUI/SGMII
- 9.5 KB
- 73
- / FIFO
- 802.1q VLAN
-
-

1.1.2

- PFC(802.1Qbb)
- ETS(802.1Qaz)
- QCN(802.1Qau)
- VEPA
- ETAG
- MIB RMON
- VXLAN/Geneve/NVGRE

1.1.3

- IPv4 TCP RSC
- FCOE
- TCP 256KB
- Linksec
- IPSec
- IP/TCP/UDP/STCP
- UDP
- CRC
- VLAN Tag
- MAC / VLAN
-

1.1.4

- MSI / MSI-X
-
- TCP
- TPH/FLR/IDO/ARI/VPD/ECRC
- 256B / 2KB
- PCIE
- D0 D3 ACPI

1.1.5

- SR-IOV
- 128
  - 32
  - 2
- 128
  - LLI
- 64 64 x 2
  63
  - 128 MAC
  - 4096
  - 4096
-

1.1.6

- 8 VLAN L2
- 16 L4
- 4 TCO
- 4 L3 Ipv4
- /
- NCSI
- 4 L3 Ipv6
- 4 L2

1.1.7

- 10 Gb
- PCIe Gen3 ———x1 x2 x4 x8
- LAN 8 GPIO
- LAN 1 IIC
- SPI
- UART
- NCSI
- 8 GPIO
- SMbus
-

1.2

Note: the single-ended signal IO level standard of WX1820AL chip is 1.8V LVCMOS standard.

Table1:Chip status

Ball #	Pin Name	Type	Description
H5	PCIE_BSY	Output Active-High	Asserted when PCI Express link has traffic
B1	ETH_UP_1		Asserted when Ethernet port1 is UP
C1	ETH_1G_0		Asserted when Ethernet port0 is at 1Gbps
D1	ETH_100M_0		Asserted when Ethernet port0 is at 100Mbps
E1	ETH_BSY_1		Asserted when Ethernet port1 has traffic
A2	ETH_10G_0		Asserted when Ethernet port0 is at 10Gbps
B2	ETH_BSY_0		Asserted when Ethernet port0 has traffic
C2	ETH_10G_1		Asserted when Ethernet port1 is at 10Gbps
D2	ETH_100M_1		Asserted when Ethernet port1 is at 100Mbps
E2	ETH_UP_0		Asserted when Ethernet port0 is UP
G4	ETH_1G_1		Asserted when Ethernet port1 is at 1Gbps
G5	MNG_BSY		Asserted when on-chip has traffic.

Table2:Chip Control

Ball #	Pin Name	Type	Description
M1	PORST_N	Input	Active-Low power-on reset
J4	PLL_BYPASS		Active-High. If asserted, Internal PLL is bypassed. It should not be asserted for normal operation.
J5	PLL_REF_CLK		50MHz PLL reference clock.

Table3:Ethernet Port0 PHY

Ball #	Pin Name	Type	Description
A4	ETH0_RX_N_0	Input	CML differential signal, Ethernet Port0 PHY differential pairs, ETH0_RX_0 differential pair for connection to SFI RX, ETH0_TX_0 differential pair for connection to SFI TX.
B4	ETH0_RX_P_0	Input	
D4	ETH0_TX_N_0	Output	
E4	ETH0_TX_P_0	Output	

Table5:PCI Express

Ball #	Pin Name	Type	Description
Y1	PE_WAKE	Output	WAKE# signal defined Input PCI Express
Y2	PERST_N	Input	PCI Express asynchronous reset
T11	PE_REF_CLK_P	Input	PCI Express 100MHz reference clock
U11	PE_REF_CLK_N	Input	
V4	PE_TX_P_0	Output	CML differential signal, PCI Express PHY differential pairs.
W4	PE_TX_N_0	Output	
AA4	PE_RX_P_0	Input	
AB4	PE_RX_N_0	Input	
V6	PE_TX_P_1	Output	
W6	PE_TX_N_1	Output	
AA6	PE_RX_P_1	Input	
AB6	PE_RX_N_1	Input	
V8	PE_TX_P_2	Output	
W8	PE_TX_N_2	Output	
AA8	PE_RX_P_2	Input	
AB8	PE_RX_N_2	Input	
V10	PE_TX_P_3	Output	
W10	PE_TX_N_3	Output	
AA10	PE_RX_P_3	Input	
AB10	PE_RX_N_3	Input	
V12	PE_TX_P_4	Output	
W12	PE_TX_N_4	Output	
AA12	PE_RX_P_4	Input	
AB12	PE_RX_N_4	Input	
V14	PE_TX_P_5	Output	
W14	PE_TX_N_5	Output	
AA14	PE_RX_P_5	Input	
AB14	PE_RX_N_5	Input	
V16	PE_TX_P_6	Output	
W16	PE_TX_N_6	Output	
AA16	PE_RX_P_6	Input	
AB16	PE_RX_N_6	Input	
V18	PE_TX_P_7	Output	
W18	PE_TX_N_7	Output	
AA18	PE_RX_P_7	Input	
AB18	PE_RX_N_7	Input	

Table6:SPI Flash

Ball #	Pin Name	Type	Description
E20	SPI_CLK_DIV_0	Input	They create a 3-bit bus. Its value determines the SPI clock (250MHz/X, where X is determined by these three signals): 1. □ □ 2. □ 3. 4. □ 5. □ Hz 6. □ 7. □ □
D22	SPI_CLK_DIV_1		
D21	SPI_CLK_DIV_2		
B20	SPI_CLK	Output	SPI Interface from SP to Flash
C20	SPI_SO	Output	
C21	SPI_SI	Input	
C22	SPI_CS_N	Output	

Table7:UART

Ball #	Pin Name	Type	Description
J2	UART_STX	Output	UART Interface to on-chip CPU
J3	UART_SRX	Input	

Ball #	Pin Name	Type	Description
T1	LAN1_GPIO_7		

Table9:MNG GPIO

Ball #	Pin Name	Type	Description
R21	MNG_GPIO_0	BiDir	Universal input and output pin of internal embedded CPU, if not used can be left unconnected.
R19	MNG_GPIO_1		
P18	MNG_GPIO_2		
P19	MNG_GPIO_3		

Table13:MDIO

Ball #	Pin Name	Type	Description
U1	MD1_CLK	Output	Used to control external PHY if SP is using external PHY.
V2	MD1_IO	BiDir	
U3	MD0_CLK	Output	
T3	MD0_IO	BiDir	

Table14:MNG SMBus

Ball #	Pin Name	Type	Description
J1	MNG_IC_DATA	OD	SMBus to on-chip CPU
K1	MNG_IC_SMBALERT_N	Output	
K3	MNG_IC_SMBSUS_N	Output	
K5	MNG_IC_CLK	OD	

Table15:Probe

Ball #	Pin Name	Type	Description
E22	PRB_EN	Input	Testing signals. They are not used Input normal
D20			operations.

Ball #	Pin Name	Type	Description
H22	PRB_DATA_21		
H19	PRB_DATA_22		
G22	PRB_DATA_23		
H18	PRB_DATA_24		
G21	PRB_DATA_25		
G18	PRB_DATA_26		
G20	PRB_DATA_27		
F22	PRB_DATA_28		
F20	PRB_DATA_29		
F21	PRB_DATA_30		
F19	PRB_DATA_31		

Table16:JTAG

Ball #	Pin Name	Type	Description
W20	JTAG_SEL_0	Input	JTAG signals for testing purpose. They are not used Input normal operations.
W21	JTAG_SEL_1	Input	
Y20	JTAG_SEL_2	Input	
Y22	JTRST_N	Input	
W22	JTDO	Output	
U19	JTMS	Input	
V20	JTDI	Input	
AA20	JTCK	Input	

Table17:Test Signals

Ball #	Pin Name	Type	Description
AB2	SCAN_ENABLE	Input	Test signals. They are not used Input normal operations.
AA1	TEST_SEL		
V1	TEST_MODE_0		
W1	TEST_MODE_1		
AA2	TEST_MODE_2		
K2	CLK_TST_SEL_0		
L4	CLK_TST_SEL_1		
L1	CLK_TST_SEL_2		
L3	CLK_TST_SEL_3		

Table18:Power Supplies

Ball #	Pin Name	Description
A1 AB1 H2 L2 P2 U2 A3 B3 C3 D3 E3 V3 W3 Y3 AA3 AB3 C4 F4 K4 N4 U4 Y4 A5 B5 C5 D5 E5 F5 U5 V5 W5 Y5 AA5 AB5 C6 F6 R6 U6 Y6 A7 B7 C7 D7 E7 R7 U7 V7 W7 Y7 AA7 AB7 C8 F8 G8 L8 N8 U8 Y8 A9 B9 C9 D9 E9 K9 M9 P9 V9 W9 Y9 AA9 AB9 C10 F10 G10 J10 L10 N10 T10 U10 Y10 A11 B11 C11 D11 E11 K11 M11 P11 R11 V11 W11 Y11 AA11 AB11 C12 F12 J12 L12 N12 T12 U12 Y12 A13 B13 C13 D13 E13 K13 M13 P13 V13 W13 Y13 AA13 AB13 C14 F14 G14 J14 L14 N14 U14 Y14 A15 B15 C15 D15 E15 K15 M15 P15 R15 U15 V15 W15 Y15 AA15 AB15 C16 F16 H16 R16 U16 Y16 A17 B17 C17 D17 E17 F17 G17 H17 R17 T17 U17 V17 W17 Y17 AA17 AB17 C18 F18 T18 U18 Y18 A19 B19 C19 D19 E19 G19 K19 N19 T19 V19 W19 Y19 AA19 AB19 A20 AB20 A21 B21 E21 H21 L21 P21 U21 AA21 AB21 A22 B22 AA22 AB22	VSS_D_0P9	Ground for digital 0.9V
K8 J9 L9 K10 J11 L11 K12 J13 L13 K14 J15 L15	VDD_D_0P9	Power supply for digital 0.9V. It must be always ON.
M8 P8 N9 M10 P10 N11 M12 P12 N13 M14 P14 N15	VDDM_D_0P9	Power supply for digital 0.9V that can be shutdown Input low power state.
J8	VSS_A_0P9	Ground for analog 0.9V
J6 K6 L6 M6 N6 P6 J17 K17 L17 M17 N17 P17	VSS_D_1P8	Ground for digital 1.8V
J7 K7 L7 M7 N7 P7 J16 K16 L16 M16 N16 P16	VDD_D_1P8	Power supply for digital 1.8V
H8	VDD_A_1P8	Power supply for analog 1.8V
H9 H10 F11 G11 H11 G12 H12 H13 H14 H15	VP_ETH_A_0P9	Power supply for analog 0.9V used by Ethernet PHY.
G6 G7 G15 G16	VPH_ETH_A_1P8	Power supply for analog 1.8V used by Ethernet PHY.
R8 T8 R9 T9 R10 R12 R13 T13 R14 T14	VP_PE_A_0P9	Power supply for analog 0.9V used by PCI Express PHY.
T6 T7 T15 T16	VPH_PE_A_1P8	Power supply for analog 1.8V used by PCI Express PHY.
H6	TEMPSENSOR_VSSA	1.8V Ground dedicated for temperature sensor
H7	TEMPSENSOR_VDDA	1.8V Power supply dedicated

VDDIO 1.8V	8.5mA	14.1mA	14.3mA	9.5mA	9.7mA	9.9mA
VDD1.8 1.8V (VPH+VDDA18)	662mA	701mA	780mA	657mA	698mA	780mA

Table20

35 ° C PN 50 ° C PN
70 ° C 0.9V 1.8V 1.1 PN 115 ° C
0.9V 1.8V 1.5

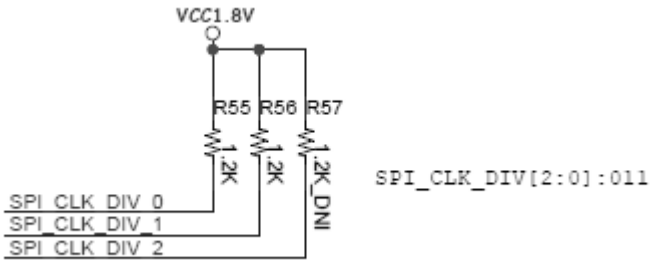
1.3.4

WOL NCSI

aux_pwr_det

WX1820AL CLK_TST_SEL_0, CLK_TST_SEL_1 CLK_TST_SEL_2 CLK_TST_SEL_3 clk_tst_sel[3:0]=0000 LAN 156.25MHZ

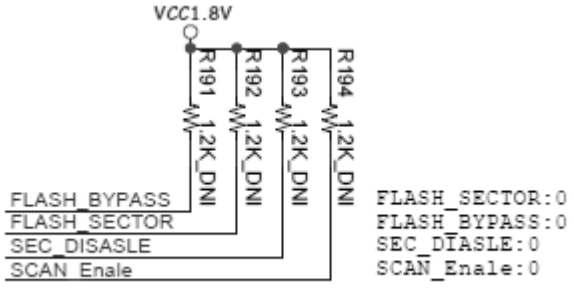
WX1820AL SPI_CLK_DIV_0 SPI_CLK_DIV_1 SPI_CLK_DIV_2 SPI_CLK_DIV[2:0]=011,SPI flash 31.25MHZ



WX1820AL TEST_MODE_0 TEST_MODE_1 TEST_MODE_2 TEST_SEL test_mode[2 :0]=000 test_sel=0

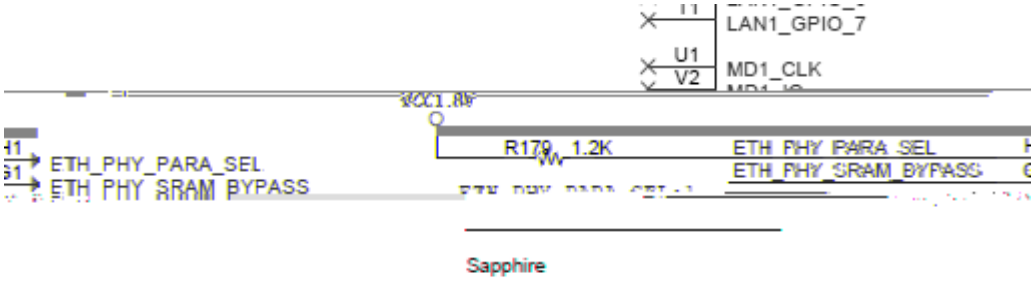
WX1820AL FLASH_BYPASS BYPASS FLASH_SECTOR SEC_DISASBLE PLL_BYPASS SEC_MODE

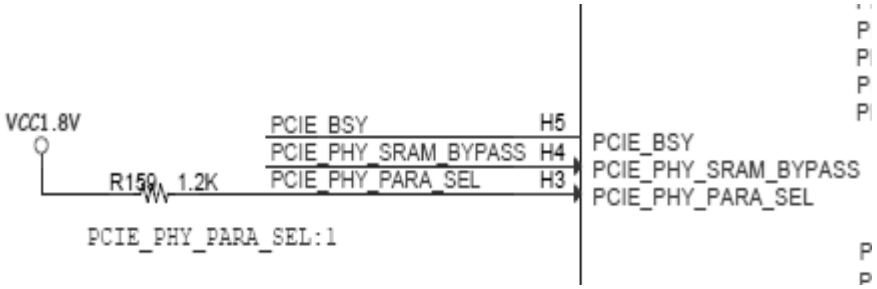
,



WX1820AL JTAG_SEL[2 :0] JTAG

WX1820AL ETH_PHY_PARA_SEL PCIE_PHY_PARA_SEL



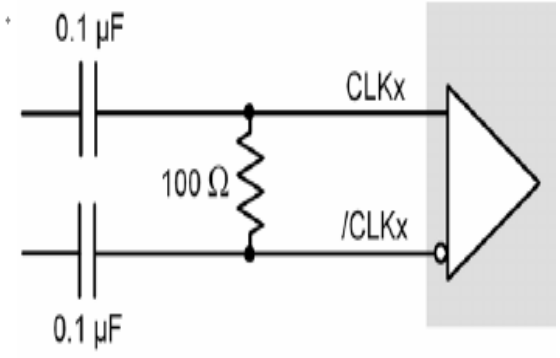


WX1820AL PCIE_PHY_SRAM_BYPASS ETH_PHY_SRAM_BYPASS LAN1_DIS_N LAN2_DIS_N

WX1820AL ETH0_RESREF ETH1_RESREF PE_PHY0_RESREF PE_PHY1_RESREF 1% 200

1.3.5 ETH

ETH0_REF_CLK_P ETH0_REF_CLK_N 156.25MHZ ETH1_REF_CLK_P ETH1_REF_CLK_N 156.25MHZ 1.8V LVDS AC DC LVDS ETH0_REF_CLK_P ETH0_REF_CLK_N ETH1_REF_CLK_P ETH1_REF_CLK_N 100 1% AC



1.3.6

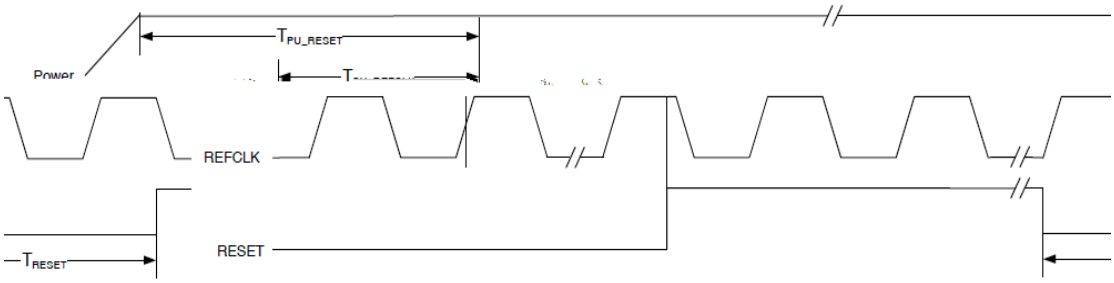
WX1820AL 0.9V 1.8V PHY VP_PE\VP_ETH 0.9V VPH\VDDA18 1.8V BLM21PG300SN1 10nF\100nF\4.7uF\10uF\47 uF 0.9V 8A 1.8V 1.5A 5W

1.3.7

WX1820AL

TPU_RESET(RESET)	10			ms
TRESET	10			ms

Table21



1.3.8 NCSI AC Specification

The WX1820AL is designed to support the standard DMTF NCSI interface. For NCSI I/F timing specification see the following table.

Tckf	NCSI_REF_CLK Frequency		50		MHz
Rdc	NCSI_REF_CLK duty cycle	35		65	%
Racc	NCSI_REF_CLK accuracy			100	ppm
Tco	Clock-to-out (10 pF =< cload <=50 pF) NCSI_RXD[1:0], NCSI_CSR_DV Data valid from NCSI_REF_CLK rising edge	3		4	ns

Tsu	NCSI_TXD[1:0], NCSI_TX_EN Data Setup to NCSI_CLK_IN rising edge	3			ns
Thold	NCSI_TXD[1:0], NCSI_TX_EN Data hold from NCSI_REF_CLK rising edge	1			ns
Tor	NCSI_RXD[1:0], NCSI_CSR_DV Output Time rise	0.5		6	ns
Tof	NCSI_RXD[1:0], NCSI_CSR_DV Output Time fall	0.5		6	ns
Tckr/Tckf	NCSI_REF_CLK Rise/Fall Time	0.5		3.5	ns

1.3.9 FLASH

bVcbX	
a WcW d	GGH 6
UX W	8

Table22 SPI FLASH

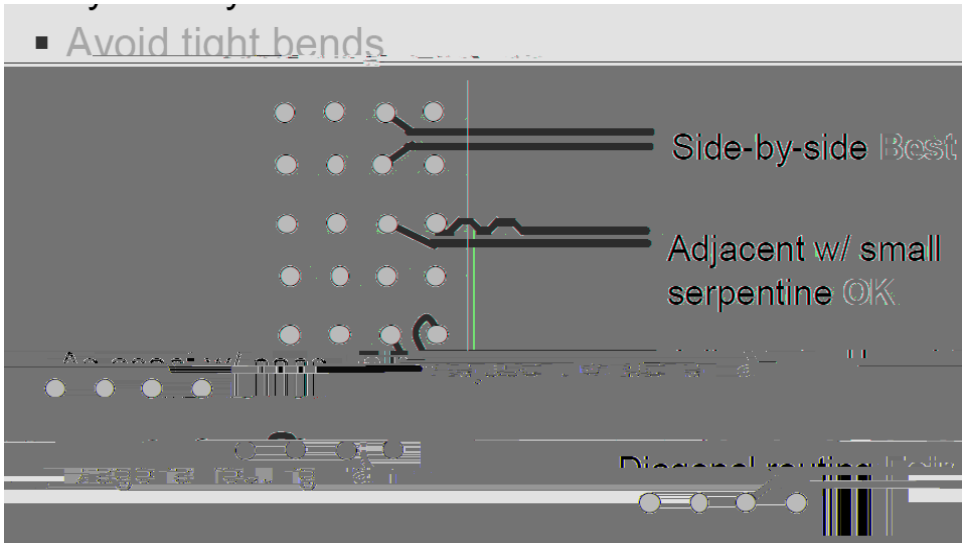
1.3.10

5 U c	5 6F!+ -GA
bh	H L + 8 67J! H
!hcb	H7G! L! 8l l
b gU	H L + 8 67
H l cb	HDG!H A ! 87F
i U	CAL8
D	GF G D - !
Ug bg	H !67
8GI	D FL D !G7!G
H8	FHL A !

Table23

1.3.11 PCI_Express

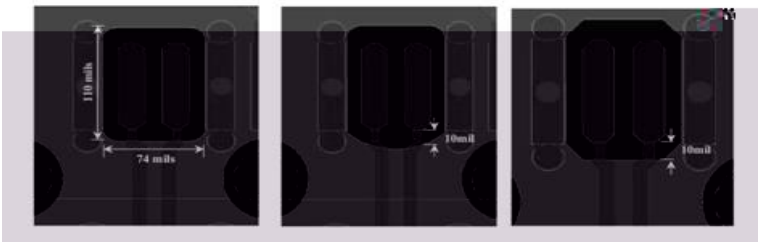
- PCI_Express 8Gbps
- 0.22uF
- 3mil
- 3W
- 2 TX RX <2000mil



1.3.12 SFP+

- SFP SFP_RX SFP_TX 5mil 50mil 2900-4000mil 3000-4000mil. 100 , 50 ,TX RX
- SFI TX RX 2

- SFP VCC3.3V 1A
- SFP
- SFI TX RX



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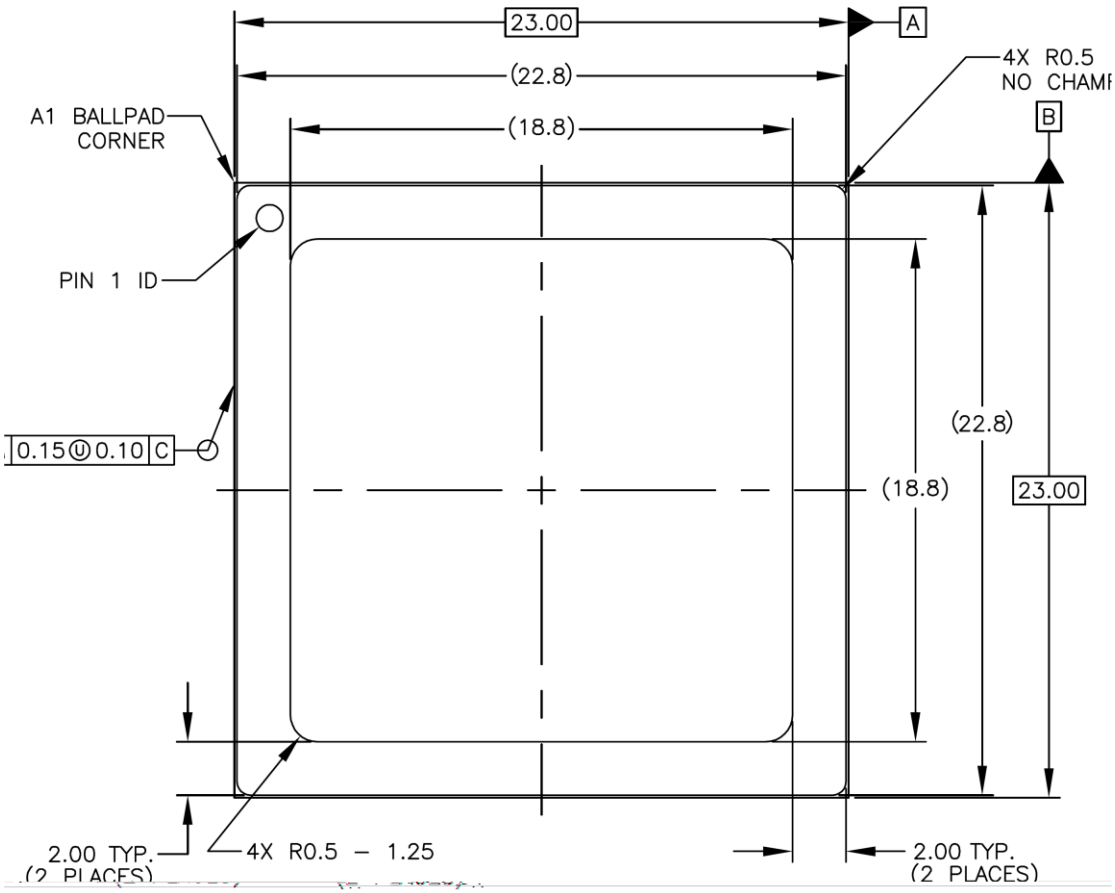
23.00
A
(22.8)
4X R0.5
NO CHAMF
(18.8)
B
A1 BALLPAD
CORNER
PIN 1 ID
0.15Ⓜ0.10 C
(22.8)
(18.8)
23.00
2.00 TYP.
(2 PLACES)
4X R0.5 – 1.25
2.00 TYP.
(2 PLACES)

TOP VIEW

6GI